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2E[15]-1 TERA BITS PER SECOND (TBPS) PRBS HDL ASIC IP DESIGN

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ABSTRACT

The Design is mainly Intended for High Speed Random Frequency Carrier Wave Generator of Tbps Data Rate using 2e15-1 Tapped PRBS Pattern Sequence. The PRBS is Designed by using LFSR Linear Feed Back Shift Register & XOR Gate with Specific Tapping Points as per CCITT ITU Standards. RTL Design Architecture Implemented by using VHDL &/ Verilog HDL, Programming & Debugging Done by using Spartan III FPGA Kit. Transmission done through this carrier frequency. Propagation Carrier Done either Serially / Parallel lines I/O.

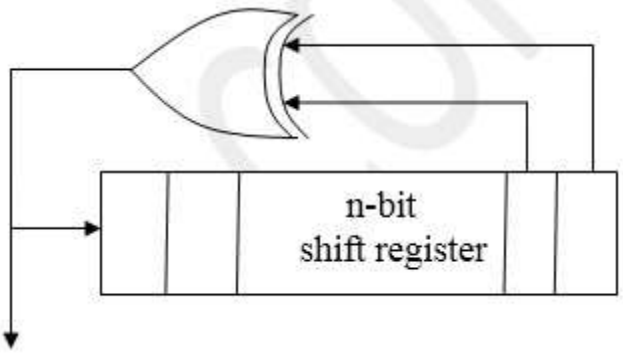
KEYWORDS: CCITT – Consulting Committee for International Telegraph & Telecom , ITU – International Telecom Unit, RTL- Register Transfer Level, LFSR-Linear Feedback Shift Register, VHDL- Very High Speed Integrated Circuit Hardware Description Language, PRBS-Pseudo Random Binary Sequence.

INTRODUCTION

In Modern Hi-tech Communication Engineering world, High Speed based Portable Communication System Hardware & Software Products Came to the market, speed is an important factor and is in terms of Giga bits per second for all Hi-tech Real time Smart Computing Portable wireless Communication System Software products like Cloud Computing ,wireless Internet Data Packets Transceivers Computing, Tablets,Pocket Mobile Multimedia Systems,NoteBookComputers,WirelessRouters,NOCs,NetworkCards/Racks,WiFI,GiFi,Wimax,GPS,GSM, QCDMATranceivers.For that purpose ,I Designed Giga Bits Per Second,Tera Bits Per Second & Peta Bits Per Second High Speed PRBS is Pseudo Random Binary Sequence Frequency Generators, Generate & Received Random Frequency Data in the form of Random frequency numbers of different speed w.r.t specific data tapping sequence points for both signal & carrier wave generation. PRBS Generators, Receivers, Transceivers Designed for HiFi Wireless Internet Data Packets Computing and Cloud Computing etc. Transmission, Reception of Data is in the RANDOM Sense, This PRBS Generator, Receiver is Designed for Identification property of Different Tapped PRBS Sequences like 7,10,15,23,31 at a Clock carrier frequency speed of Gbps/Tbps/Pbps.the Length of PRBS sequence is 2L-1. 2L-1 times repeated the sequences. this is mainly suit for multiple users to transmit and received data in accurate time for very long distance communications like GPS Data Acquisition, GSM Communication Systems, WiFI,GiFI,LTE, Wireless OFDMA , CDMA,QCDMA Computing, wireless internet computing, cloud computing etc because of Ultra High speed Communication Rate in terms Gbps,Tbps,Pbps . All these PRBS LFSR Sequences are designed by tapping different points according to ITU O.150,O.151,O.152 Standards. This PRBS Design Consists of Multiplexer, PRBS Registers of different tapped sequence points, Clock Frequency Generators of Gbps/Tbps/Pbps Speed. The Advantages of these PRBS Generators having In Built Checkers, Bit Error Rate Detection & Correction by using PRBS Checkers. these are simply Linear Polynomial Checkers & CRC.

with minimum number of taps and XOR gate in its feedback.

FIG[1]: Fibonacci (many-to-one) realization of LFSR



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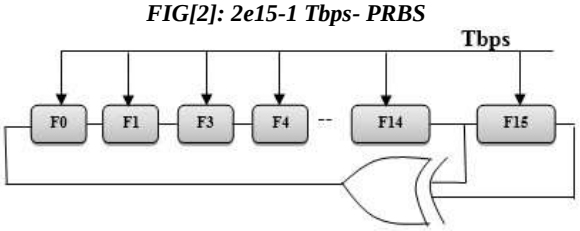
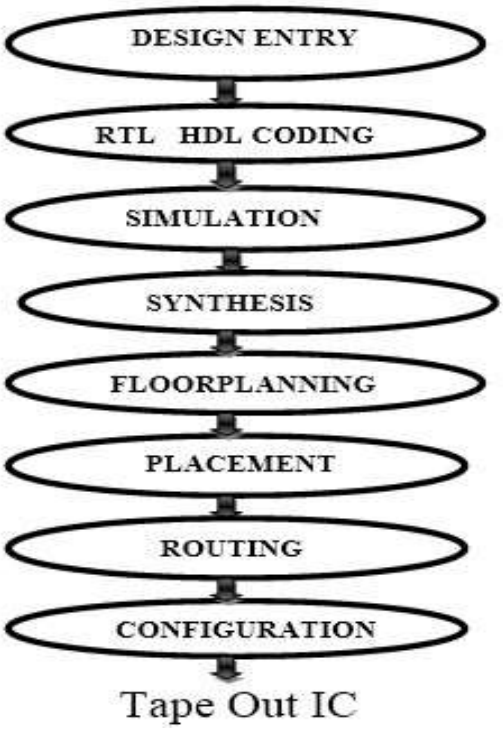
2E15-1 TBPS- PRBS DESIGN

FIG[2]: 2e15-1 Tbps- PRBS



SOFTWARE – VLSI IC DESIGN FLOW



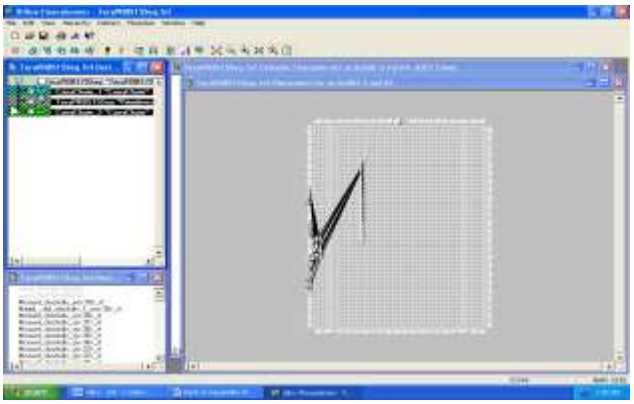
FIG[3]: VLSI Design Flow Chart

DESIGN FLOW REPORTS OF 2e15-1 Tbps PRBS DESIGN

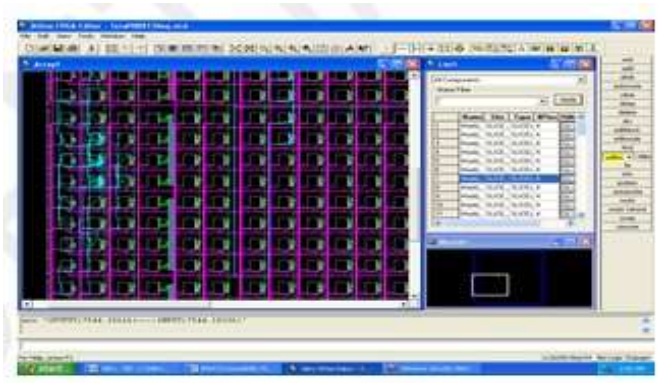
2e15-1 Tbps PRBS DESIGN RTL BLOCK

RTL Schematic

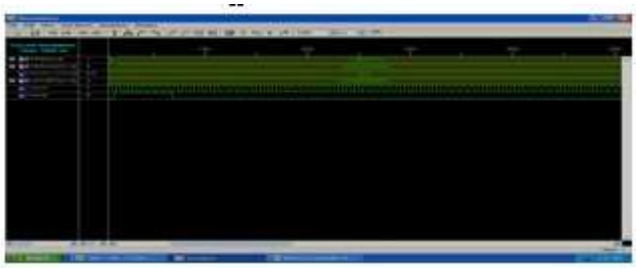
DESIGN PLACED REPORT



Design Routed Report



SIMULATION WAVE FORM RESULTS



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CONCLUSION

Designed 2e15-1 Tbps PRBS for Ultra High Speed Wireless Communications, This Design is mainly intended for Ultra Very High Long Distance Communication at the frequency rate of Tera Bits per Second. And this product is very suited for All Very Advanced Smart Digital Computing Communication Products like Advanced 3G,4G,5G,6G, Hi-Fi Space Communication ,Satellite Communication Products.

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